Advance Product Information

July 26, 2007

2-20 GHz LNA/Gain Block

TGA2513-SM

Key Features

- Frequency Range: 2-20 GHz
- 17 dB Nominal Gain
- 16 dBm Nominal P1dB
- 2.5 dB Midband Noise Figure
- Bias Conditions: Vd=5V, Idq=75 mA, Vg2=2V
- Package Dimensions: 4.0 x 4.0 x 0.9 mm

Primary Applications

- Wideband Gain Block / LNA
- X-Ku Point to Point Radio
- IF & LO Buffer Applications

Product Description

The TriQuint TGA2513-SM is a packaged LNA/Gain Block. The LNA operates from 2-20 GHz and is designed using TriQuint's proven standard 0.15 um gate pHEMT production process.

The TGA2513-SM provides a nominal 16 dBm of output power at 1 dB gain compression with a small signal gain of 17 dB. Typical noise figure is < 3 dB from 2-15 GHz.

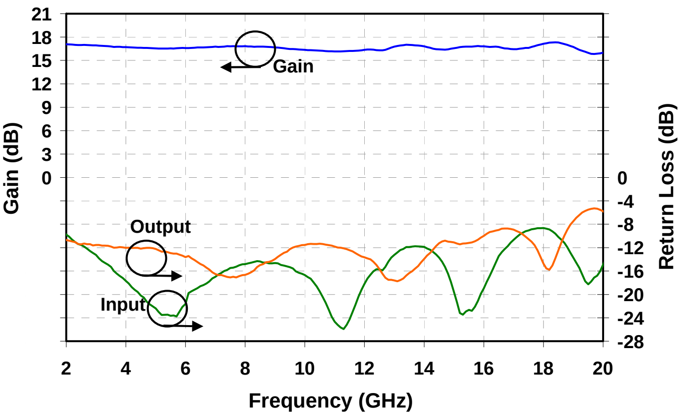
The TGA2513-SM is suitable for a variety of wideband electronic warfare systems such as radar warning receivers, electronic counter measures, decoys, jammers and phased array systems.

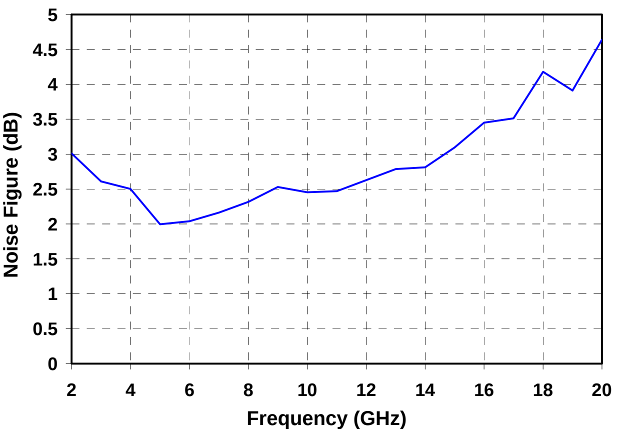
Evaluation Boards are available upon request.

Lead-free and RoHS compliant

Measured Performance

Bias Conditions: Vd = 5 V, Idq =75 mA, Vg2 = 2V





Note: This device is early in the characterization process prior to finalizing all electrical specifications. Specifications are subject to change without notice.

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
Vd	Positive Supply Voltage	5 V	2/
Vg1	Gate 1 Supply Voltage Range	-1V to 0 V	
Vg2	Gate 2 Supply Voltage Range	(Vd – 3) to (Vd – 2) V	
Id	Positive Supply Current	151 mA	2/
| Ig |	Gate Supply Current	10 mA	
P_{IN}	Input Continuous Wave Power	21 dBm	2/
P_D	Power Dissipation	See note 3	2/, 3/
T_{CH}	Operating Channel Temperature	117 °C	4/
T_M	Mounting Temperature (30 Seconds)	260 °C	
T_{STG}	Storage Temperature	-65 to 117 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Current is defined under no RF drive conditions. Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ For a median life time of 1E+6 hrs, Power dissipation is limited to:

$$P_D(max) = (117\ °C – Tbase\ °C) / 32\ (°C/W)$$

4/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
RF CHARACTERIZATION TABLE
(T_A = 25 °C, Nominal)
Vd = 5V, Id = 75 mA Vg2 = 2V Vg1 = ~ -60 mV

SYMBOL	PARAMETER	TEST CONDITION	NOMINAL	UNITS
Gain	Small Signal Gain	f = 2-20 GHz	17	dB
IRL	Input Return Loss	f = 2-20 GHz	12	dB
ORL	Output Return Loss	f = 2-20 GHz	10	dB
NF	Noise Figure	f = 2-20 GHz	3	dB
P_{1dB}	Output Power @ 1dB Gain Compression	f = 2-20 GHz	16	dBm

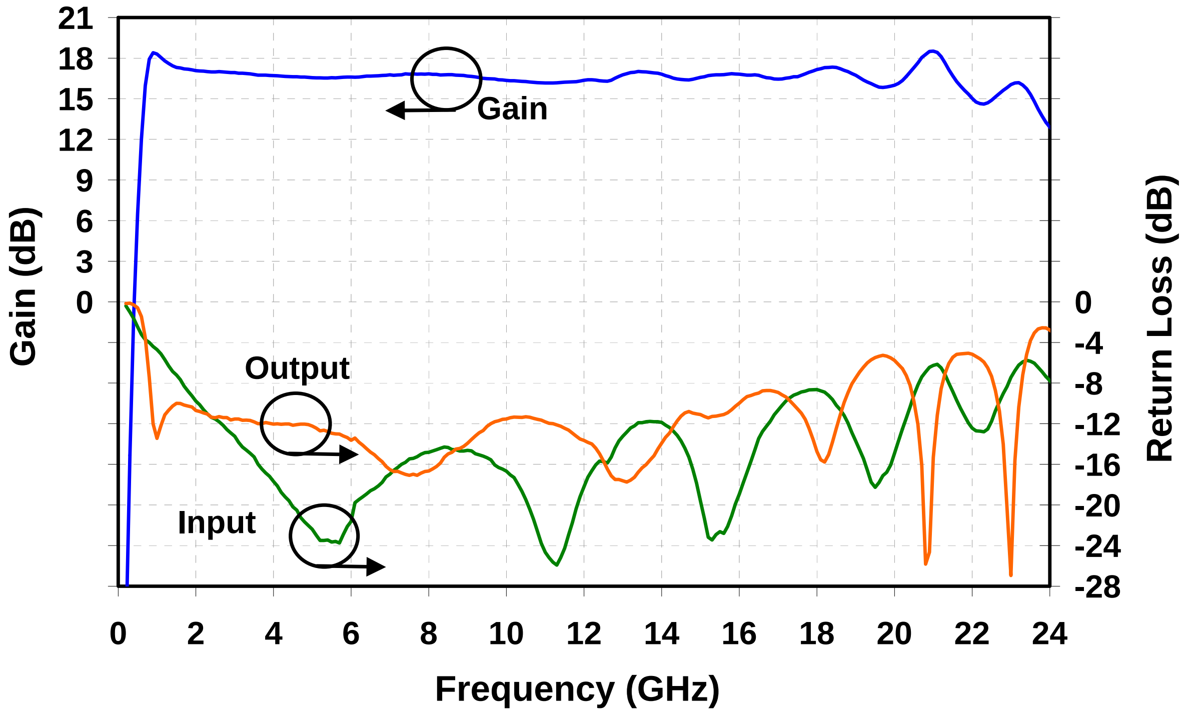
TABLE III
THERMAL INFORMATION

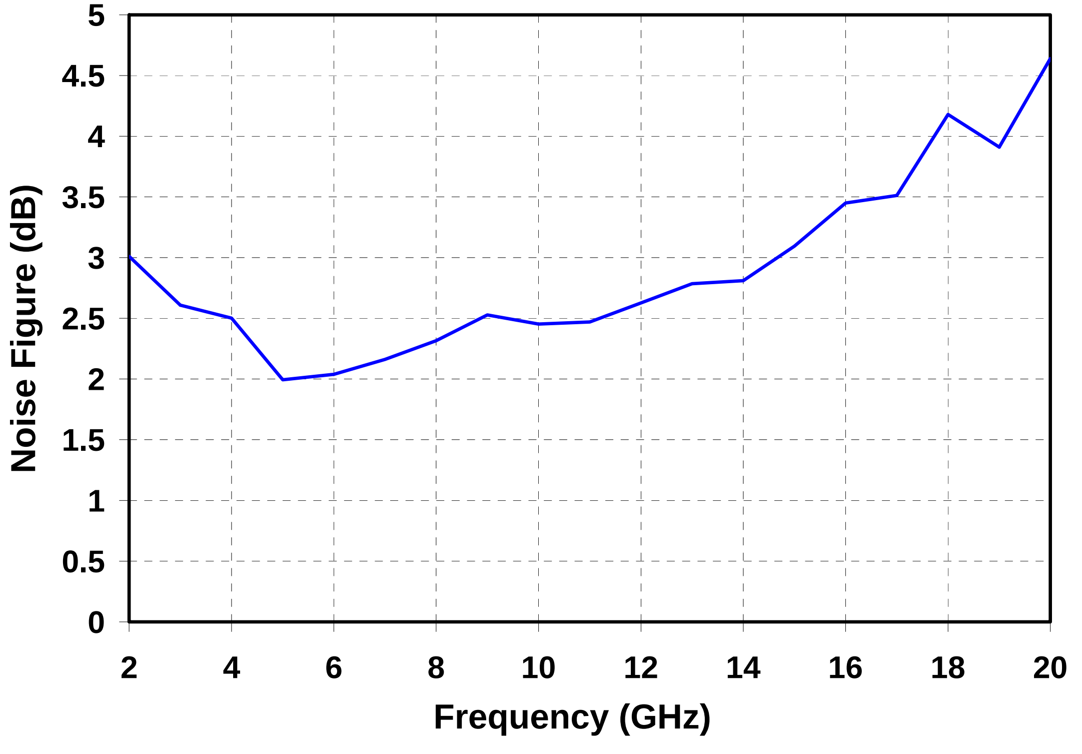
Parameter	Test Conditions	T_{CH} (°C)	θ_{JC} (°C/W)	T_M (HRS)
θ_{JC} Thermal Resistance (channel to backside of carrier)	Vd = 5 V Id = 75 mA Pdiss = 0.375 W	97	32	8.1 E+6

Note: Worst case condition with no RF applied, 100% of DC power is dissipated. Package temperature @ 85 °C

Measured Performance

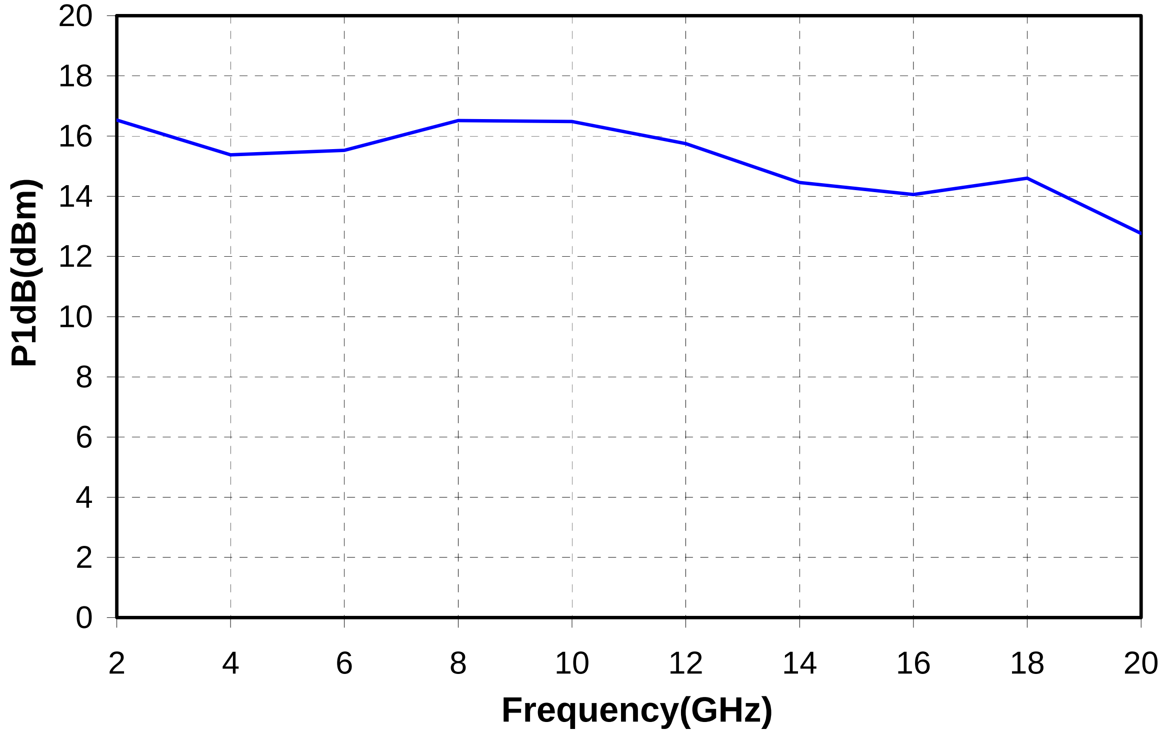
Bias Conditions: Vd = 5 V, Idq =75 mA, Vg2 = 2V, Vg1 = ~-60mV, typical

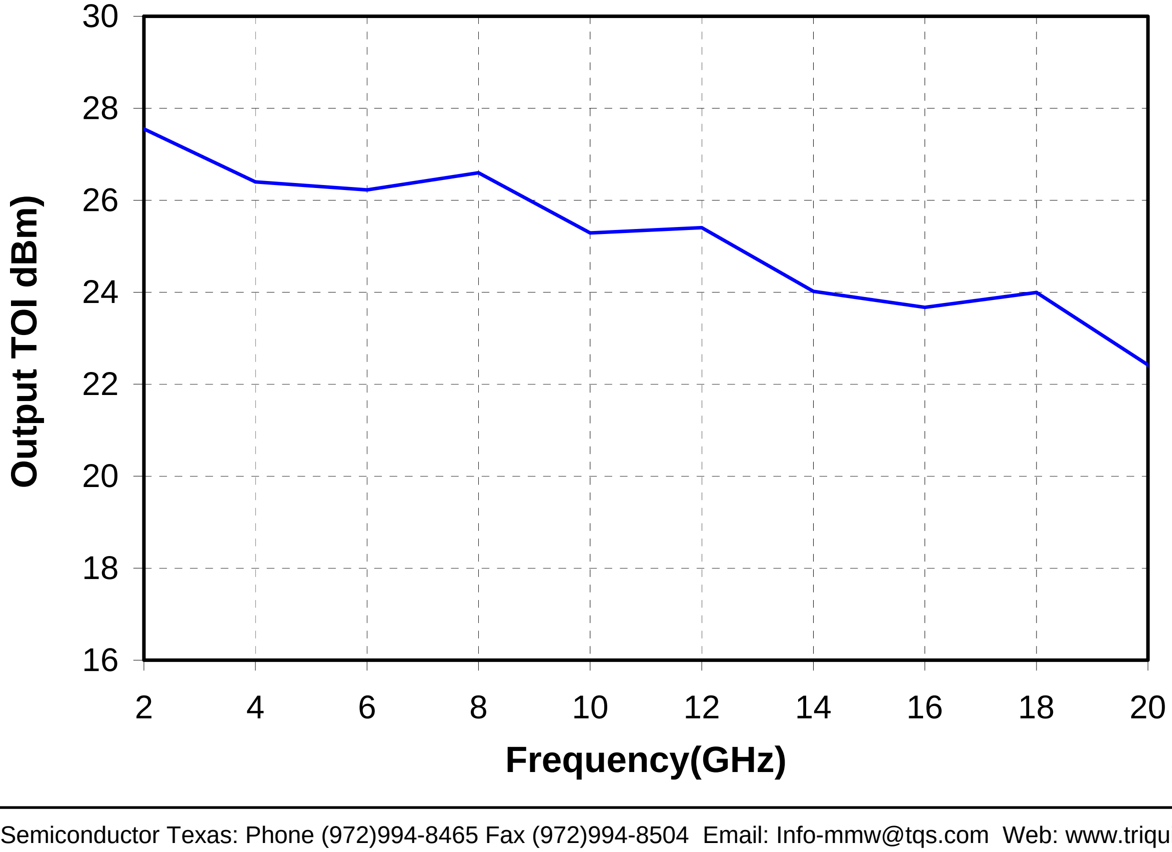




Measured Performance

Bias Conditions: Vd = 5 V, Idq =75 mA, Vg2 = 2V, Vg1 = ~-60mV, typical





Measured Performance

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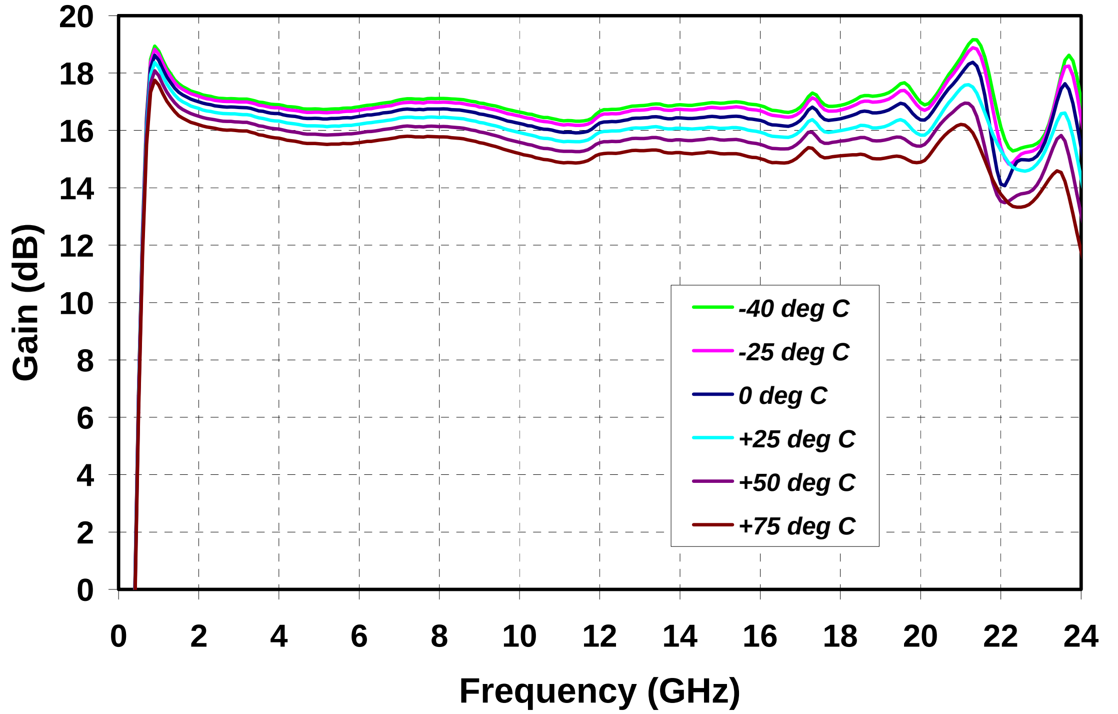
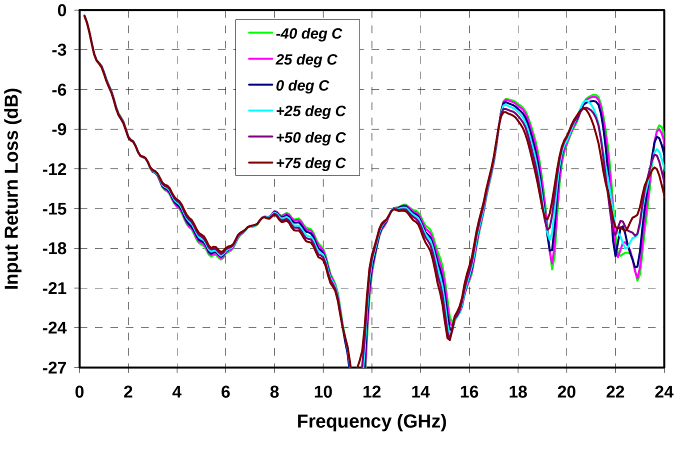
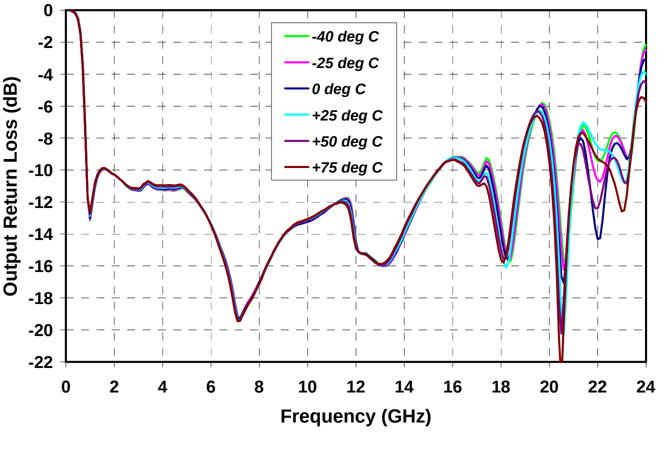
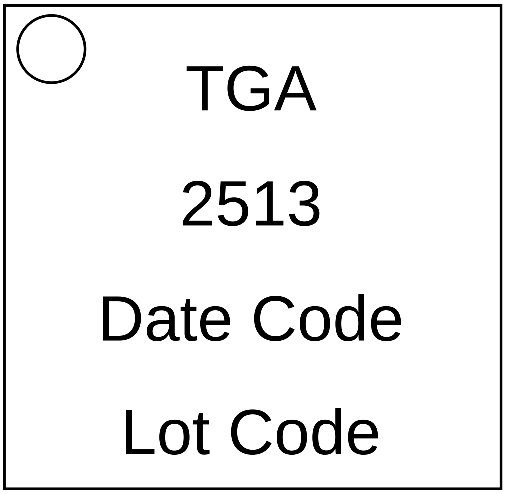






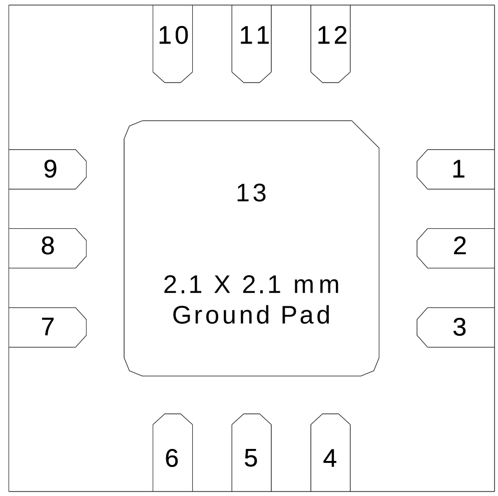
Measured data is taken using connectorized evaluation boards. The reference plane is at RF connectors, and hence connector and board loss has not been de-embedded.

Package Pinout Diagram



Top View

Dot indicates Pin 1



Bottom View

Pin	Description
1, 3, 4, 5, 7, 8, 10, 13	Ground
2	RF Input
6	Vg1
9	RF Output
11	Vd
12	Vg2

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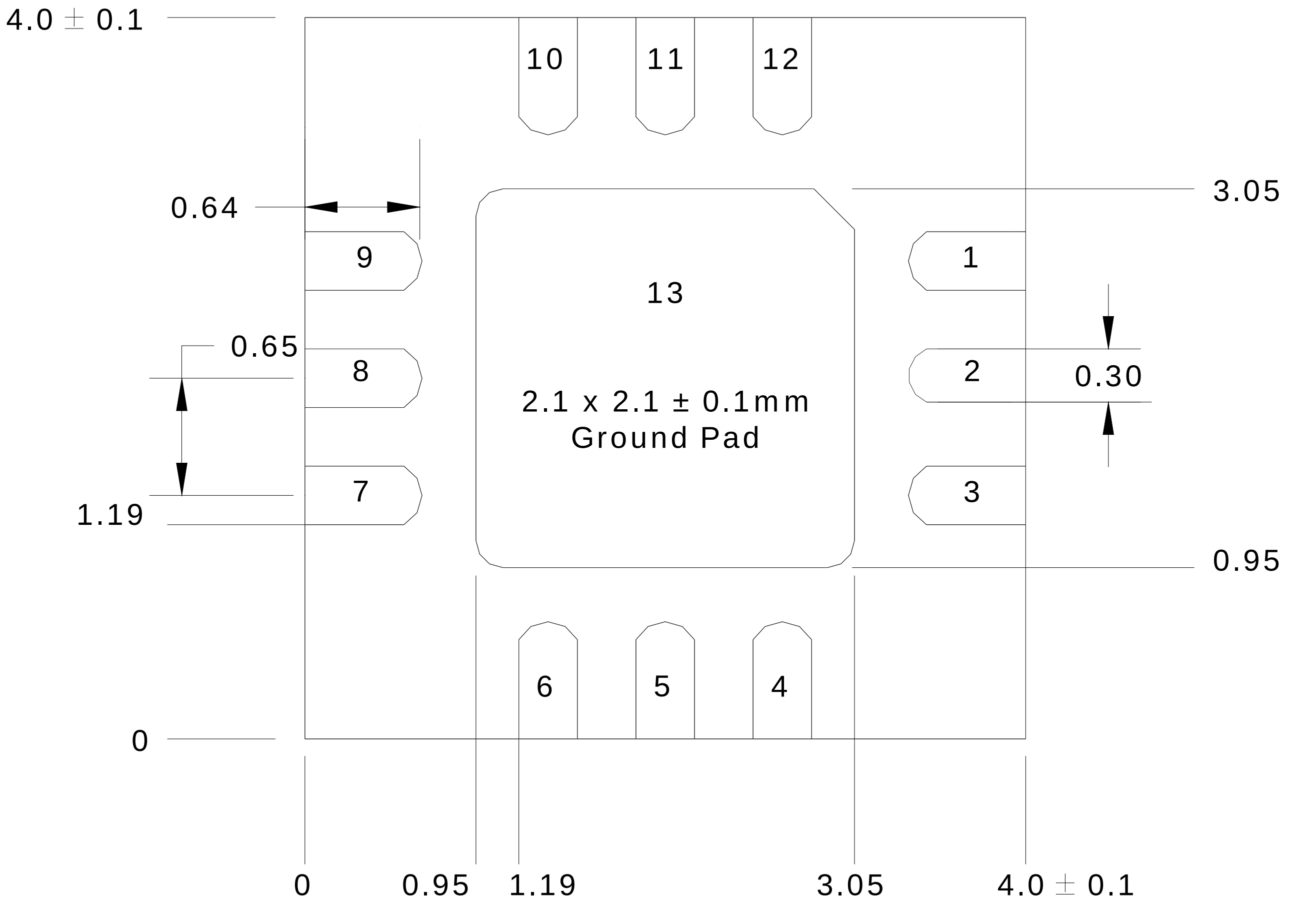
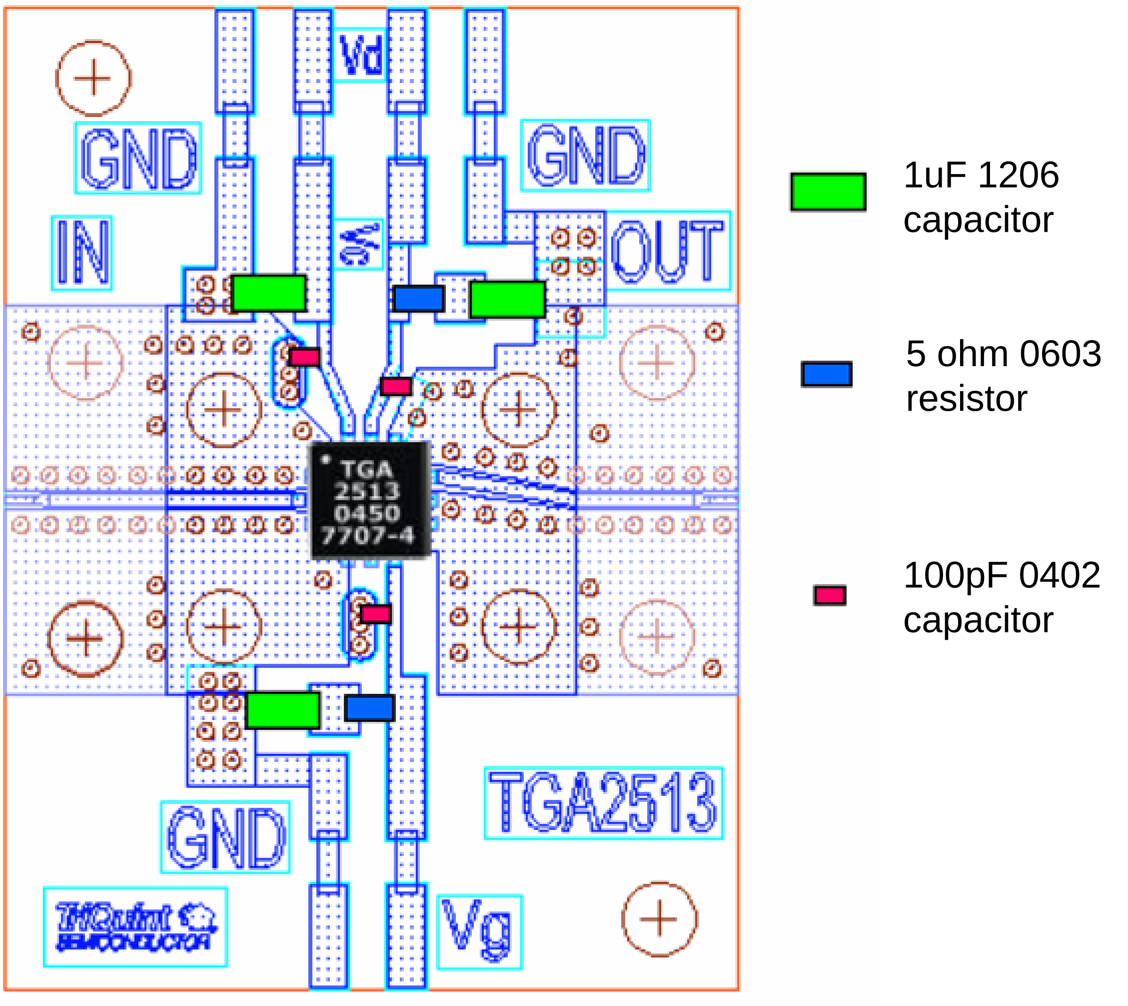
Mechanical Drawing



Bottom View
Tolerance: +/- 0.05
Units: mm

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Recommended Board Layout Assembly



Recommended Bias-up Procedure

1. Ensure no RF power is applied to the device
2. Pinch-off device by setting Vg (Vg1) to -1V
3. Increase Vd to 5V while monitoring gate current
4. Increase Vc (Vg2) to 2V
5. Increase Vg (Vg1) until drain current reaches 75 mA
6. Apply RF Power

Recommended Bias-Down Procedure

1. Turn off RF power
2. Decrease Vg (Vg1) to -1V
3. Decrease Vc (Vg2) to 0 V
4. Decrease Vd to 0 V

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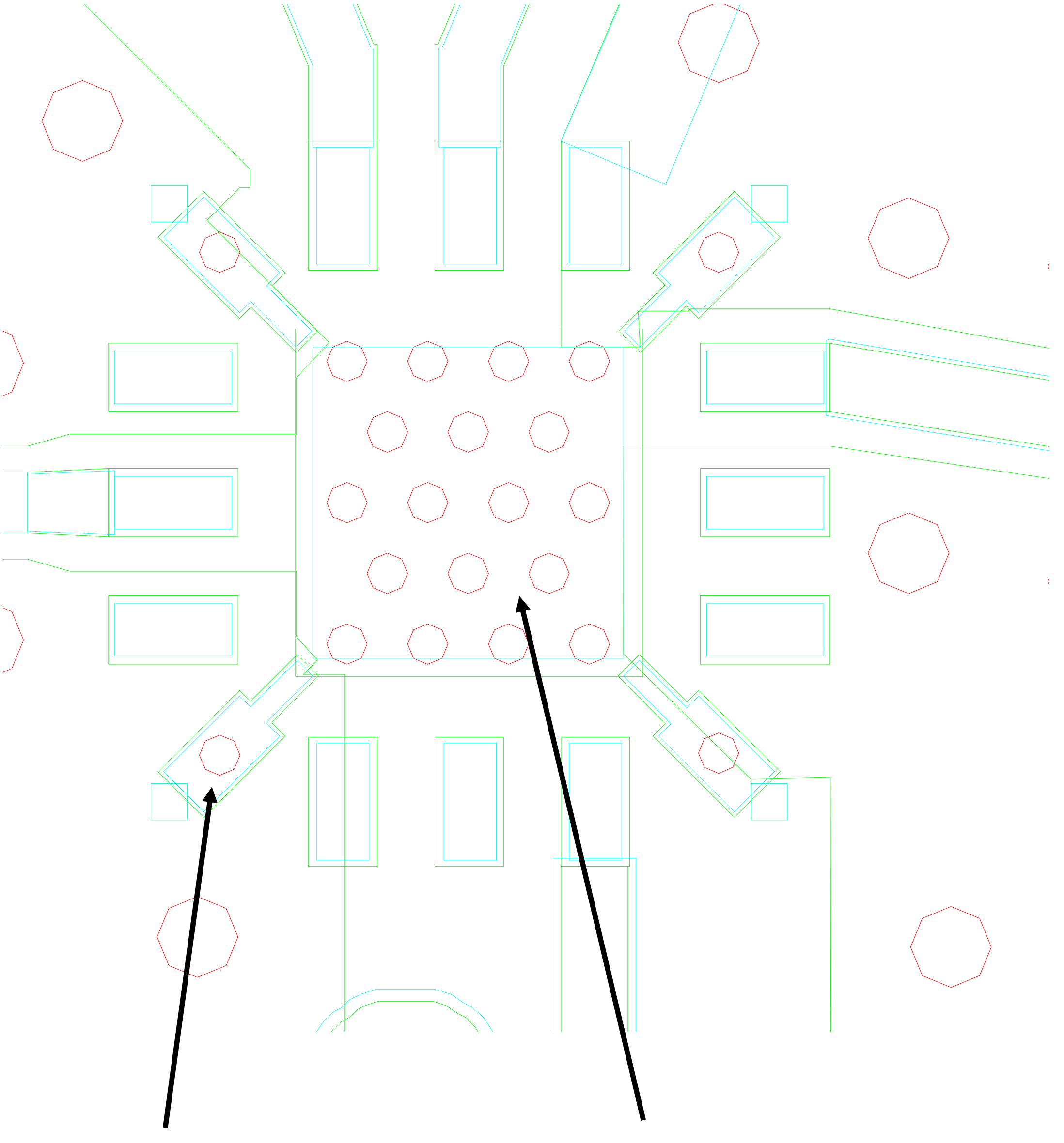
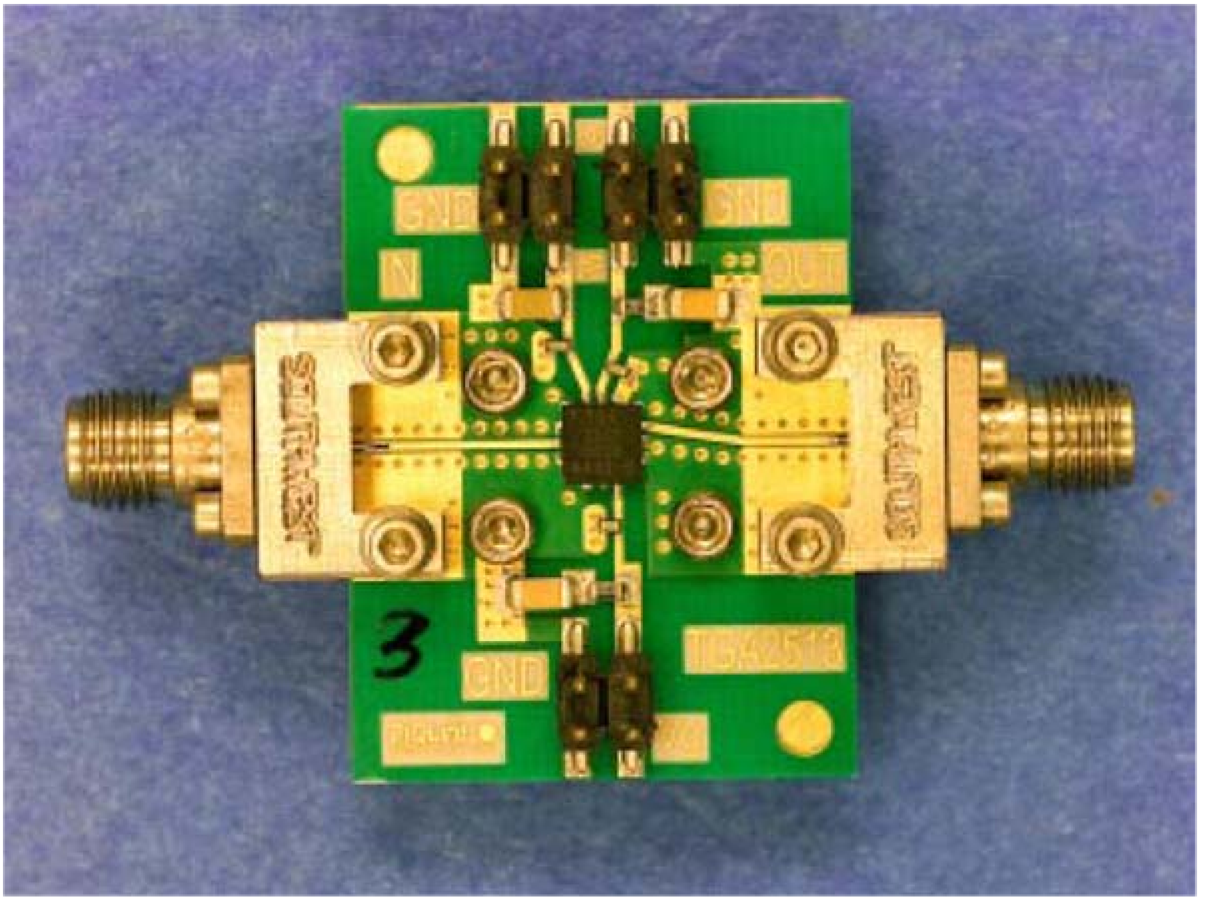
Evaluation Board Layout Details



Via holes in the four corners of the package are required to ensure stable operation. These vias need to be connected to ground paddle

Maximum density of via holes under ground paddle for optimum electrical and thermal performance

TGA2513-SM Evaluation Board



Evaluation Board is Rogers RO4003
8mil thickness
0.5oz standard copper cladding
dielectric constant (Er) = 3.38

Recommended Surface Mount Package Assembly

Proper ESD precautions must be followed while handling packages.

Clean the board with acetone. Rinse with alcohol. Allow the circuit to fully dry.

TriQuint recommends using a conductive solder paste for attachment. Follow solder paste and reflow oven vendors' recommendations when developing a solder reflow profile. Typical solder reflow profiles are listed in the table below.

Hand soldering is not recommended. Solder paste can be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance.

Clean the assembly with alcohol.

Typical Solder Reflow Profiles

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

Ordering Information

Part	Package Style
TGA2513-SM	QFN 12L 4x4 Surface Mount

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